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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/564,454

05/10/2006

Dirk Soenksen

RECP:114US

8959

24041 7590 01/07/2009
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EXAMINER

CHAWAN, SHEELA C

ART UNIT

PAPER NUMBER

2624

MAIL DATE

DELIVERY MODE

01/07/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/564,454	Applicant(s) SOENKSEN ET AL.	
	Examiner SHEELA C. CHAWAN	Art Unit 2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 10-14 is/are rejected.
- 7) ☒ Claim(s) 4-9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Preliminary Amendment

2. Preliminary amendment filed on 1/12/06 has been entered.

Drawings

3. The Examiner has approved drawings filed on 1/12/06.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim(s) 1-14 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. Supreme Court precedent¹ and recent Federal Circuit decisions² indicate that a statutory “process” under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing. While the instant claim(s) recite a series of steps or acts to be performed, the claim(s) neither transform underlying subject matter nor positively tie to another statutory

¹ *Diamond v. Diehr*, 450 U.S. 175, 184 (1981); *Parker v. Flook*, 437 U.S. 584, 588 n.9 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 70 (1972); *Cochrane v. Deener*, 94 U.S. 780, 787-88 (1876).

² *In re Bilski*, 88 USPQ2d 1385 (Fed. Cir. 2008).

category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 10 -14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamey, Jr. et al., (US. 6,408,219 B2), in view of by Tanaka (US. 6,973,209 B2).

As to claim 1, Lamey, discloses a method for teaching a knowledge-based database for automatic defect classification (abstract, fig 2, element 28 and 30), which comprises:

(a) selecting review data file (column 2, lines 11-13, 24 - 39, column 10, lines 36 - 60, column 11, lines 38- 49);

(b) inputting parameters and data by a user on one page of a learning mode wherein the parameters and the data are known to the user (column 5, lines 39- 45);

(c) starting an alignment procedure and a procedure for adjusting light intensity (column 5, lines 7-28);

(d) automatically adjusting automatic adjustment of the optimal intensity of the lighting by approaching a few defects and if necessary regulating to the optimal illumination (column 6, lines 38- 44);

Lamey is silent about (e) checking a detection using a few examples, whereby the optimization of the detection parameters is carried out using pictures;

(f) automatically approaching_all defects of a wafer or wafers, whereby the respective defect is detected and a descriptor is assigned to the respective defect; and

(g) analyzing and automatically grouping of the descriptors of the defect.

Tanaka discloses defect inspection system which inspects defects on a surface of e.g., a semiconductor wafer. The system comprises of:

(e) checking a detection using a few examples, whereby the optimization of the detection parameters is carried out using pictures (note, fig 2, pictures corresponds to thumbnail image, column 8, lines 10-21);

(f) automatically approaching_all defects of a wafer or wafers, whereby the respective defect is detected and a descriptor is assigned to the respective defect (column 9, lines 4-24, 52-59, fig 5) ; and

(g) analyzing and automatically grouping of the descriptors of the defect (column 9, lines 25 - 47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Lamey to include the optimization of the detection parameters is carried out using pictures. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Lamey by the teaching of Tanaka in order to determine that thumbnail images obtained by minimizing the images (as suggested by Tanaka at column 2, lines 45- 51).

As to claim 2, Tanaka discloses the method according to Claim 1, wherein the input of parameters and data further comprise the selection of elements present on a semiconductor substrate, wherein the elements can be memory circuits, logic circuits, a bare blank wafer without resist or with resist (column 5, lines 5-17).

As to claim 3, Tanaka discloses the method wherein the parameters or data of layers on the wafer comprise the data of a polymer layer, an oxide layer, a contact or a metal layer (column 5, lines 5 - 14).

As to claim 10, Tanaka discloses the method according to claim 8, wherein 20 defects are used to adjust the intensity of the illumination (column 4, lines 11-23).

As to claim 11, Tanaka discloses the method according to claim 1, wherein the defects on the wafer that are automatically approached, have pictures are taken and which are temporarily stored until pictures are taken of all the defects (fig 2, column 4, lines 64- 67, column 5, lines 1-25).

As to claim 12, Tanaka discloses the method according to Claim 11, wherein after all the pictures are taken, these they are shown on a display as thumbnails (fig 2, and fig 5, column 9, lines 4 - 47).

As to claim 13, Tanaka discloses the method according to Claim 12, wherein a few thumbnails are rejected if the thumbnails exceed a threshold value for the focus (column 5, lines 1- 17, column 6, lines 12- 25, column 7, lines 28- 44).

As to claim 14, Tanaka discloses the method according to Claim 1, wherein the analysis and automatic grouping of the descriptors of the defects divides the thumbnails of the defects recorded into groups, and on the display the first nine examples of a selected group of defects are displayed in a thumbnail representation (column 5, lines 1- 17, column 6, lines 12- 25, column 7, lines 28- 44).

Allowable Subject Matter

6. Claims 4 - 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Non of the prior art on record teaches or fairly suggests the method wherein the parameters or data of layers on the wafer comprise the data of a polymer layer, an oxide layer, a contact or a metal layer as required by claim 4.

Claims 5 - 10 depend directly or indirectly on the object base claim. Therefore, they are objected for the same reason.

Other prior art cited

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lin et al. (US. 6,292,582 B1) discloses method and system for identifying defects in a semiconductor.

Gleason et al., (US. 6,456,899 B1) discloses context-based automated defect classification system using multiple morphological mask.

Han (US. 6, 104,835) discloses automatic knowledge database generation for classifying objects and system therefor.

Hennessey et al., (US. 6,483,938 B1) discloses system and method for classifying an anomaly.

Hosoya et al., (US. 6, 792,367 B2) discloses method and apparatus for inspecting defects in a semiconductor wafer.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHEELA C. CHAWAN whose telephone number is (571)272-7446. The examiner can normally be reached on 7.30- 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on 571-272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)? If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sheela C Chawan/

1/2/09

Primary Examiner, Art Unit 2624

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